IN THE SPECIFICATION

(1) Please replace the paragraph entitled "Cross Reference to Related Applications" beginning at line 2, page 1 with the following rewritten paragraph:

**CROSS REFERENCE TO RELATED APPLICATIONS**

The present invention is related to the following U.S. Patent Applications which are incorporated herein by reference:

~~Serial No. _____ (Attorney Docket No. AUS920000517US1) entitled "Multiphase Serializer" filed _____.~~

Serial No. [[_____]] 09/820,507 ~~(Attorney Docket No. AUS920000512US1)~~ entitled "Multiphase Retiming Mechanism" filed March 29, 2001 [[_____]].

(2) Please replace the paragraph beginning at line 16, page 4 with the following rewritten paragraph:

~~Figure 6 illustrates~~ Figures 6A-B illustrate an embodiment of a sample clock mechanism in a synchronization state selector unit configured in accordance with the present invention;

(3) Please replace the paragraph beginning at line 3, page 5 with the following rewritten paragraph:

Figure 1 illustrates an embodiment of the present invention of a serial data link 100 used in a communication system. As stated in the Background Information, data may typically be transmitted between various devices in a communication system through a data link. Typically, data is transmitted in parallel whenever possible in order to increase bandwidth. However, due to cost, weight, interference (noise) and electrical loading considerations, parallel transmission is not feasible in many systems. In order to simplify the communications problem, data may be

transmitted serially across a serial data link 100 by a transmitter 101. Transmitter 101 may be configured to convert the parallel data to a serial form which may be transmitted through a medium 102, e.g., wired, wireless, to a receiver 103 configured to convert the serial data into parallel form which may then be transmitted to another device, e.g., computer, cellular phone. ~~A more detailed discussion of transmitter 101 converting parallel data into serial data using multiple phases of a phase clock at a frequency lower than the serial data rate is described in detail in U.S. Application No. _____, filed on _____, entitled "Multiphase Serializer," Attorney Docket No. AUS920000517US1, which is hereby incorporated herein by reference in its entirety.~~

(4) Please replace the paragraph beginning at line 21, page 5 and ending at line 20, page 6 with the following rewritten paragraph:

Figure 2 illustrates an embodiment of the present invention of a receiver 103 configured to receive serial data 201 transmitted from transmitter 101 through medium 102, e.g., wired, wireless. Receiver may comprise a phase detector 202 configured to receive serial data 201 transmitted by transmitter 101 through medium 102, e.g., wired, wireless. Phase detector 202 may further be configured to generate N synchronization states that are inputted to retiming mechanism 205. Phase detector 202 may further be configured to generate an error signal. The functionality of phase detector 202 is described in greater detail in U.S. Publication No. 20020085657, ~~Application No. _____~~, filed on December 28, 2000 [[_____]], entitled "Multiphase Clock Recovery Using D-Type Phase Detector," ~~Attorney Docket No. AUS920000518US1,~~ which is hereby incorporated herein by reference in its entirety. The error signal generated by phase detector 202 is filtered through filter 203 which outputs a control voltage used by oscillator 204, e.g., voltage controlled oscillator, to generate N phases of a clock that is inputted to retiming mechanism 205. In one embodiment, oscillator 204 may be configured to operate at a frequency lower than the serial data rate thereby saving power. The

output of oscillator 204 is also inputted to phase detector 202 as illustrated in Figure 2. Additional details regarding the functionality of oscillator 204 is described in related U.S. Application Serial Nos. 09/726,282 and 09/726,285, both filed on November 30, 2000, which are hereby incorporated herein by reference in their entirety. Phase detector 202, filter 203 and oscillator 204, e.g., voltage controlled oscillator, may collectively be referred to as a clock and data recovery unit configured to extract a clock from the serial data stream 201 which is used to retime the data, i.e., diminish jitter, by retiming mechanism 205 as described in the description of Figures 4-8. The clock and data recovery unit is described in greater detail in U.S. Patent No. 6,441,667, issued on August 27, 2002, ~~U.S. Application No. _____, filed on _____~~, entitled "Multiphase Clock Generation," ~~Attorney Docket No. AUS920000513US1,~~ which is hereby incorporated herein by reference in its entirety.

(5) Please replace the paragraph beginning at line 15, page 10 with the following rewritten paragraph:

Figure 5 illustrates one embodiment of the present invention of a synchronization state selector unit 411. Synchronization state selector unit 411 may comprise a sample clock mechanism 501 configured to generate sampled clock phase values as will further be described in the description of ~~Figure 6~~ Figures 6A-B. That is, sample clock mechanism 501 indicates the logical state, e.g., low or high, of each phase of the clock generated by oscillator 204 at a particular point in time. Synchronization state selector unit 411 may further comprise a plurality of synchronization state detectors 502A-E configured to generate the logical state, e.g., low or high, of a particular synchronization state/retiming state pair, e.g., $SS_1RS_4$, $SS_2RS_5$, $SS_3RS_1$, $SS_4RS_2$, $SS_5RS_3$, as will be further described in the description in Figure 7. Synchronization state detectors 502A-E may collectively or individually be referred to as synchronization state detectors 502 or synchronization state detector 502, respectively. It is noted that synchronization state selector unit 411 may

comprise a different number of synchronization state detectors 502 and that Figure 5 is illustrative. Synchronization state selector unit 411 may further comprise a synchronization state completion detector 503 configured to generate a completion signal indicating the time to sample the inputs to select a particular synchronization state/retiming state pair, e.g. $SS_1RS_4$, $SS_2RS_5$, $SS_3RS_1$, $SS_4RS_2$, $SS_5RS_3$, as will be further described in the description in Figure 8.

(6) Please replace the paragraph beginning at line 6, page 11 with the following rewritten paragraph:

~~Figure 6~~ Figures 6A-B – Sample Clock Mechanism

~~Figure 6 illustrates~~ Figures 6A-B illustrate one embodiment of the present invention of a sample clock mechanism 501. Sample clock mechanism may comprise a plurality of latches 601A-J configured to sample a particular phase of the clock generated by oscillator 204 at a particular point in time. Latches 601A-J may collectively or individually be referred to as latches 601 or latch 601, respectively. It is noted that sample clock mechanism 501 may comprise a different number of latches 601 corresponding to a different number of phases of the clock generated by oscillator 204 and that ~~Figure 6 is~~ Figures 6A-B are illustrative.

(7) Please replace the paragraph beginning at line 12, page 21 with the following rewritten paragraph:

As stated above, retiming mechanism 205 may comprise a synchronization state selector unit 411A (Figure 4) configured to generate logical values for each synchronization/retiming state pair, e.g., $SS_1RS_4$, $SS_2RS_5$, $SS_3RS_1$, $SS_4RS_2$, $SS_5RS_3$, for each positive edge transition of serial data 201 and a synchronization state selector unit 411B (Figure 4) configured to generate logical values for each synchronization/retiming state pair, e.g., $SS_1RS_4$, $SS_2RS_5$, $SS_3RS_1$, $SS_4RS_2$, $SS_5RS_3$, for each negative edge transition of serial data 201. Each synchronization state selector unit 411 may comprise a sample clock mechanism 501 (Figure 5) configured

to sample the phases of the clock generated by oscillator 204 in step 903 as described in the description of ~~Figure 6~~ Figures 6A-B.

(8) Please replace the paragraph beginning at line 10, page 22 with the following rewritten paragraph:

In step 906, a particular synchronization sate/retiming state pair, e.g., $SS_1RS_4$, $SS_2RS_5$, $SS_3RS_1$, $SS_4RS_2$, $SS_5RS_3$, may be selected based on the logical values of the inputs to synchronization state detector 503 as described in the description of Figure 8. In one embodiment, a multiplexer 504 (Figure 5) may be configured to output a selected synchronization ~~sate/retiming~~ state/retiming state pair based on the logical values of the inputs to synchronization state detector 503. The one complemented input to synchronization state detector 503 that remains deasserted, i.e., low, corresponds to the particular synchronization state/retiming state asserted.

(9) Please replace the term "**CLAIMS:**" beginning at line 1, page 24 with the following:

**We Claim:**